Minerva LLC
Tomsk

Common information

minerva technology

- Founded in 2010, company brings together specialists in the field of hardware and software design. The company specializes in the development and implementation of efficient algorithms for digital signal processing and compression video / audio streams.
- Products: IP Cores for digital signal processing and video/audio compression. Xilinx FPGA based hardware development.
- The company provides services for the IP Core development, hardware and software systems design using cutting-edge techniques

Team development skills

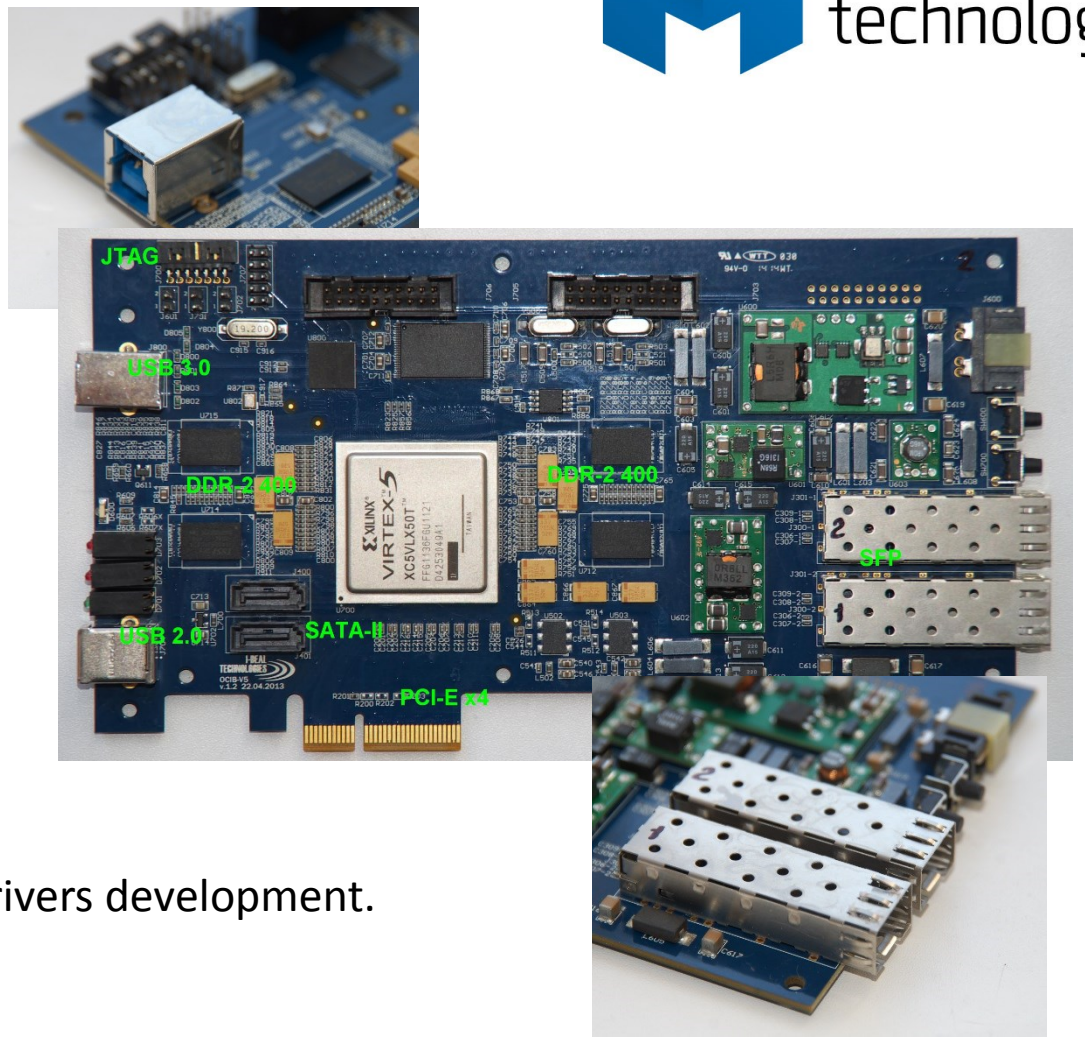
minerva technology

- Technical specification development from customer whishes
- Hardware/software architecture development. Optimizing Bill of Materials. Schematic development (digital/analog)
- Any PCB type development
- IP Core development for any FPGAs
- System and user level software development

Success story

minerva technology

- OCIB-V5
  - Board intends for control and transfer data of ultrasonic sensors array to PC
  - Interface for control and data transmission – two Optical Gigabit SFP. PC interface – PCI-Express or/and USB-3.0.
  - Bandwidth for ultrasonic sensors data - 106МБ/с (0.85Gbps). Bandwidth of PCI-Express ~ 8 Gbps (1Gbyte/s), USB 3.0 – 2.8 Gbps (350MByte/s)
  - I-Deal Technologies GmbH manufactures fastest in the world system nondestructive ultrasonic control system based on OCIB-V5

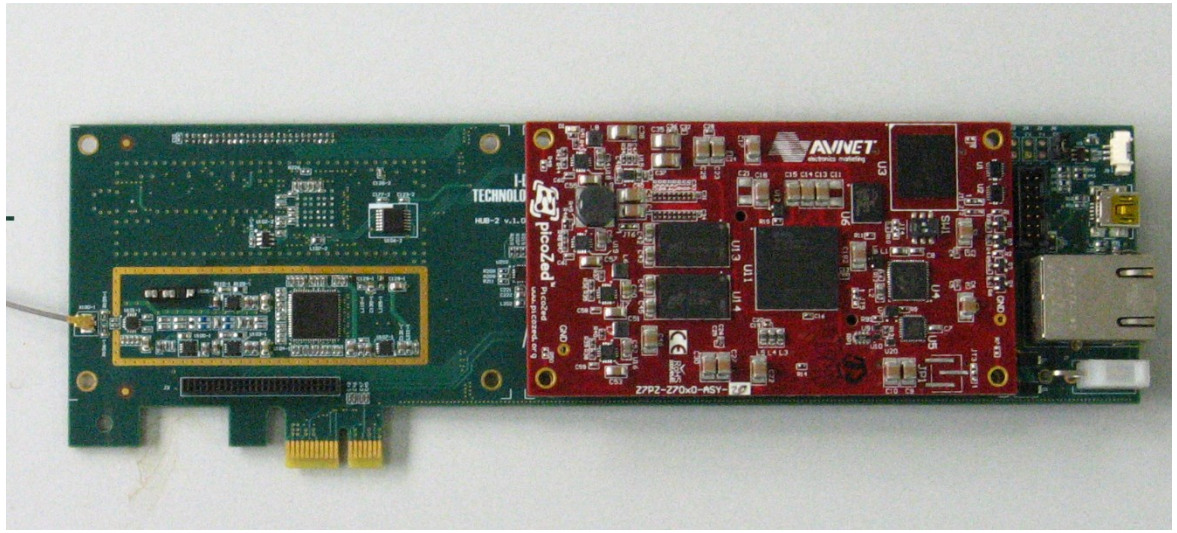


Team tasks/skills: Schematics, PCB design, HDL design, drivers development.
Customer- Fraunhofrer IFZP

Success story

minerva technology

- Two channel frontend ultrasonic sensors array for NDT system
  - Board intends for control and transfer data of ultrasonic sensors array to PC. Up to 16 boards on backplane
  - Interface for control and data transmission – 1G Ethernet
  - Bandwidth for ultrasonic sensors data – 16 bits 250 MHz ADC for one channel



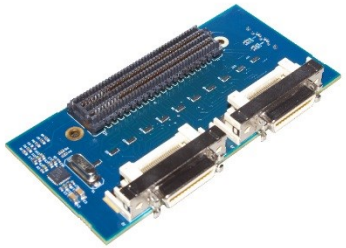
Team tasks/skills: System architecture design, schematics, PCB design, HDL design, embedded software development for carrier board and test software for server.

Customer- Fraunhofrer IFZP

Success story

- **uScio** . Minerva own project
  - USB-3.0, SFP, FMC LPC, FPGA Xilinx Spartan
  - Versatile board for capturing, storing and transferring data from/to FMS devices and PCs. Supports White Rabbit technology (CERN). http://www.minerva-tech.com/en/products/digital_connectivity_hardware/fmc_carrier

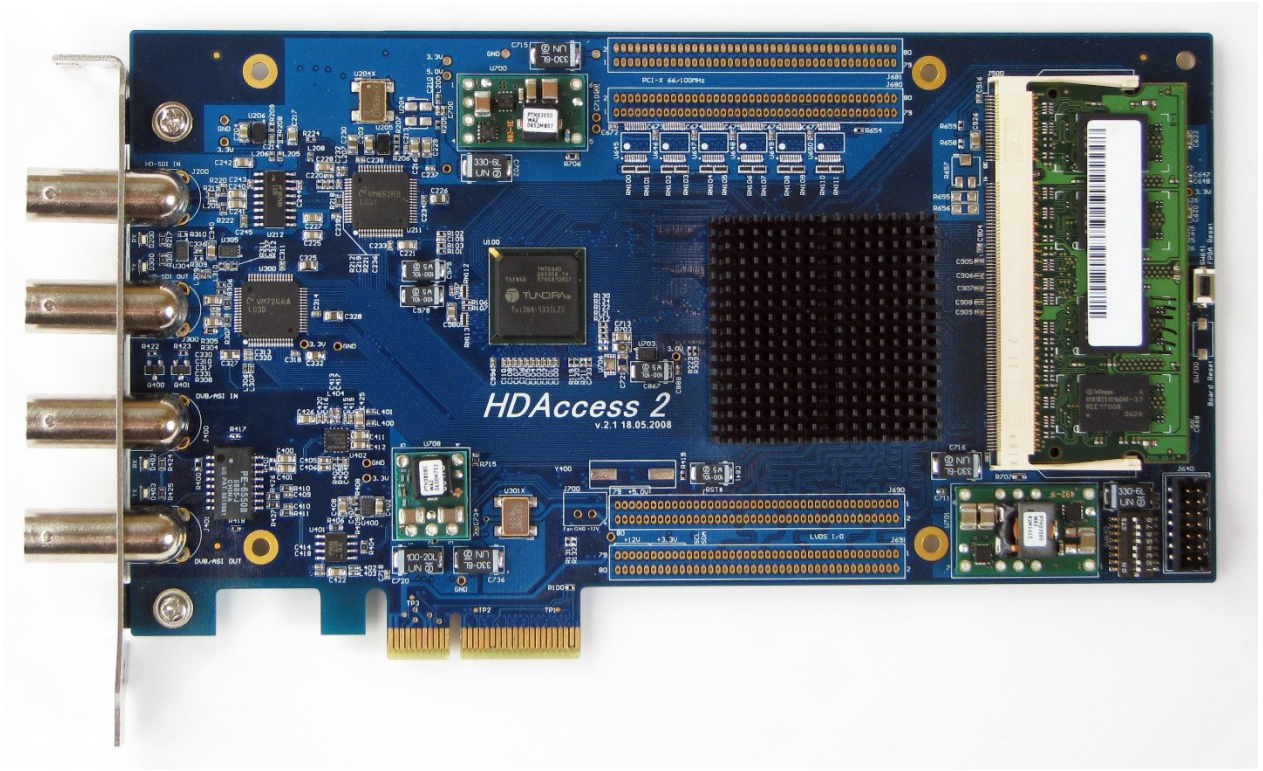
Team tasks/skills: Schematics, PCB design, HDL design, drivers development.
Customers: Tomsk State University, CSN Electronic GmbH



Success story

minerva technology

- HDAccess-2. HD SDI Video In/Out board
  - FPGA Xilinx Virtex-4, PCI-Express x4. Board captures video data from SDI with extremely low delay (<1ms).
  - Board functionality based on following IP Cores: SDI Capture, Deblock (H.264 coding standard), Denoiser, Up2HDScaller, MPEG2 TS Demultiplexer, MPEG2 TS Multiplexer.

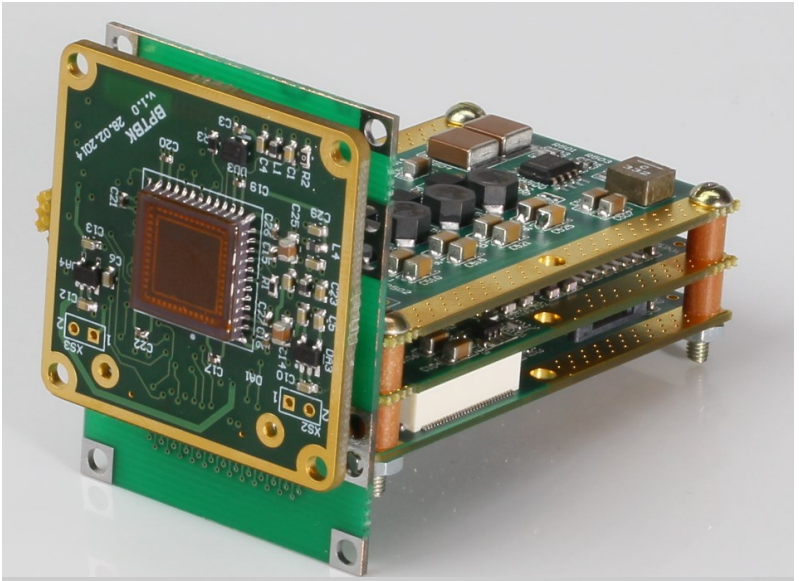


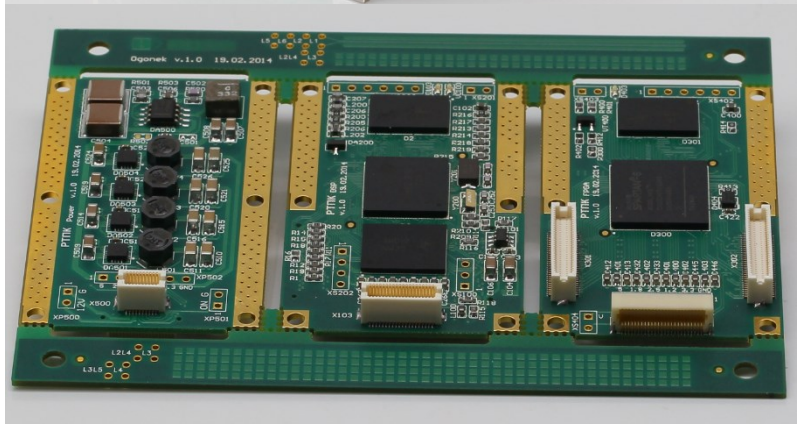
Team tasks/skills: Schematics, PCB design, algorithms, HDL design, drivers design
Customers: Elecard (www.elecard.com), GreenHippo (www.green-hippo.com)

Success story

minerva technology

- Wireless security system (special application)
  - Embedded (TI DM365) system for compression and transmission data from IR (FLIR) or Video sensor (E2V). Adaptive rate control algorithms for extremely low bandwidth (15 kbit/sec) wireless interfaces.





Team tasks/skills: Schematics, PCB design, Algorithm, HDL design, OS Linux, driver development, climatic and vibration tests, certification, preparing for mass production.
Customers: under NDA.

Success story

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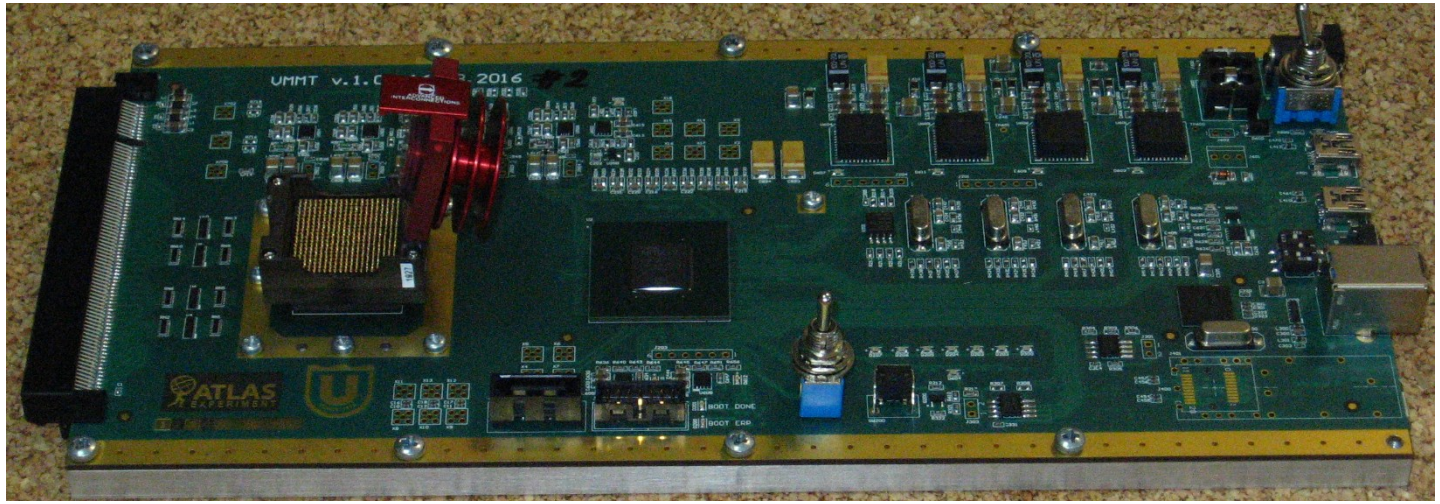
- 2GE2SFP – II level router (six 1Gbit ports)
  - Sisco style command line interface
  - Web interface

Team tasks/skills: Schematics, PCB design, OS Linux, climatic and vibration tests, certification, preparing for mass production.
Customers: Under NDA

Success story

minerva technology

- VMMT – VMM chip tester.
  - VMM – 64 channel analog/digital SoC for precise measurement amplitude and duration of output pulses
  - Need test before supplying into MM and sTGC detectors of ATLAS experiment (CERN)
  - A lot of proprietary hardware interfaces



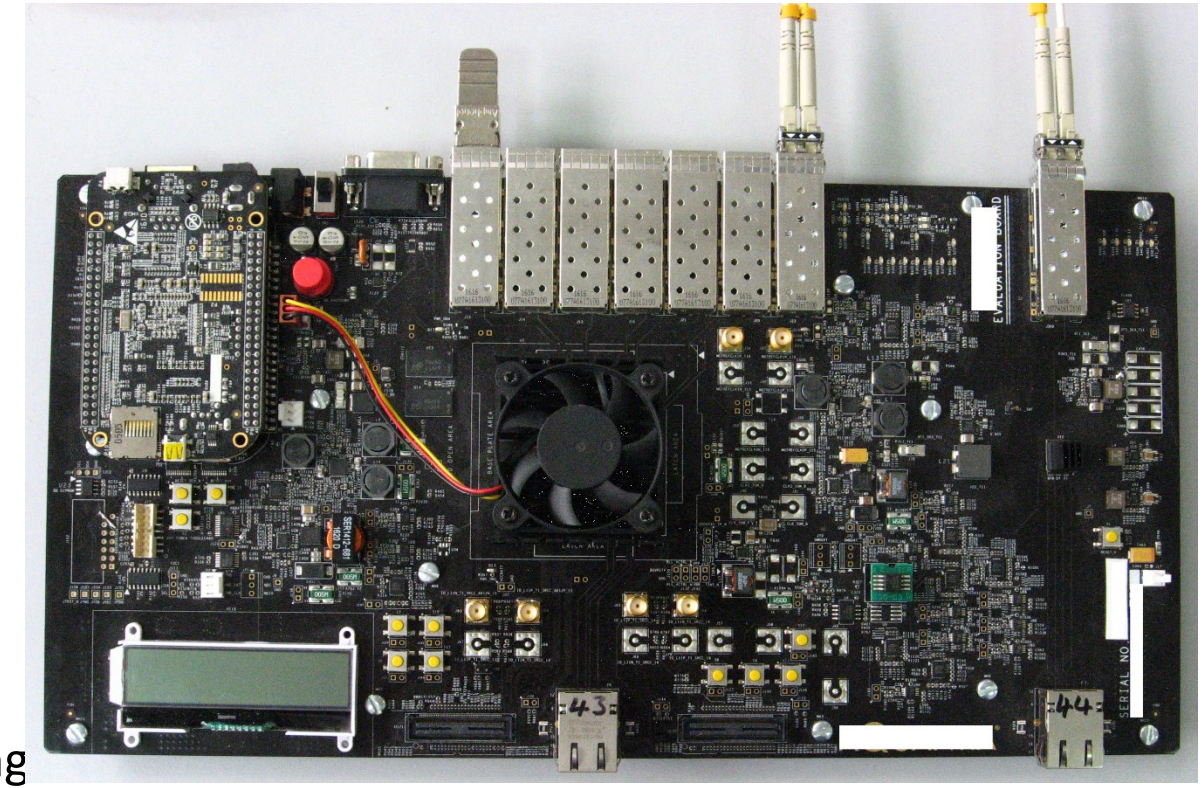
Team tasks/skills: Schematics, PCB design, HDL design, Windows user application development.

Customer: TSU for CERN (ATLAS experiment)

Success story

minerva technology

- Test code for 10G-Base-T SoP.
  - SoP – Xilinx Kintex + Aquantia 10G PHY.
  - Test code covers all SoP subsystems: BERT, eye- scan diagram for transceivers, DDR, MMCM, PLLs, FF.
  - Tests adaptation for running on the Agilent 93K test system



Team tasks/skills: HDL design, technical consulting

Customer: Under NDA

Success story

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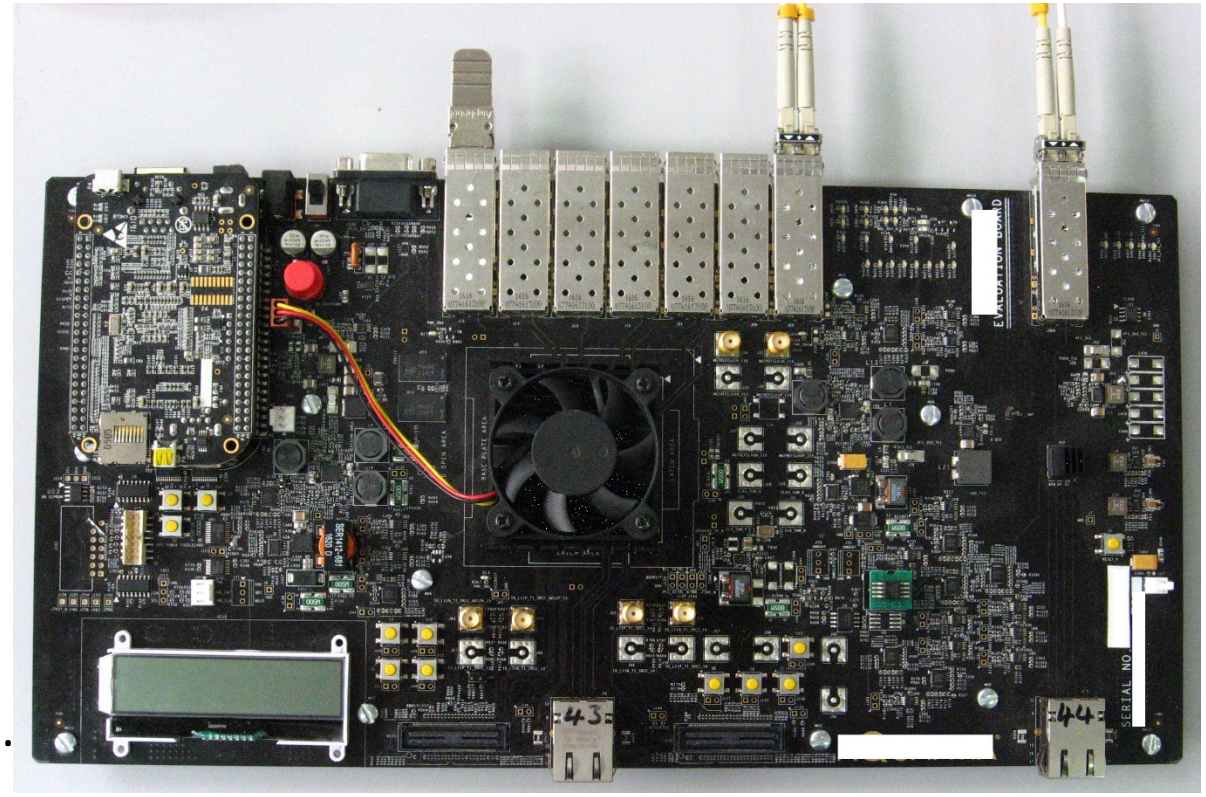
- Synchronous transmission video data over Ethernet (10G). Proof of concept development.
  - Master device transmit clock and data over Ethernet. Receivers synchronously recover master clock and payload
  - Proprietary datagram protocol development



Team tasks/skills: HDL design, technical consulting.

Customer: Under NDA

Products

minerva technology

- IP Cores
  - SATA II/III Controller – SATA interface controller
  - Video Port – video output functional block provides 2D acceleration functionality
  - UpScaler – provides high quality real-time video scaling
  - Low Latency AVC Encoder – AVC encoder IP Core with extremely low latency
  - CABAC decoder/encoder – IP Cores of CABAC (Context-adaptive Binary Arithmetic Coding) algorithm processing

  http://www.minerva-tech.com/en/products/ip_cores

Experience and knowledge

minerva technology

- Complex embedded system design.
- HDL design: VHDL, Verilog, System Verilog.
- RTL design for ASIC.
- Digital signal processing.
- Video compression expertize: AVC, HEVC.
- Development and prototyping proprietary communication system with broadband digital modulation.

Thanks for your attention!