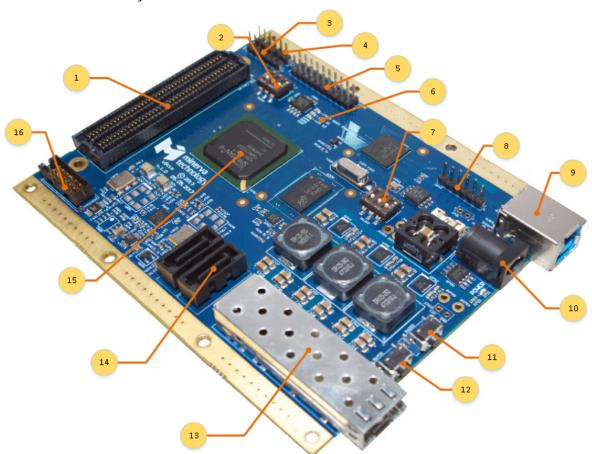


## uScio USB 3.0 FMC Carrier Board

Modern wired and wireless comunications systems, radio and geolocation systems, tomography, nondestructive testing systems and many others are based on the digital processing of the registered signals. In real systems the digital processing hardware block has to solve extremely wide range of different problems. List of problems covers both the simplest tasks of signal preprocessing and complex adaptive filtering results of digitized multidimensional fields (electromagnetic, sound, heat, etc.). Frequently, fast prototyping of this functional block allows proving possibility of realization of the measurement system as a whole.

The world's first USB 3.0 **FMC Carrier Board** provides great opportunities for rapid development a wide range of digital measurement systems. The **uScio USB 3.0 FMC Carrier Board** that is based on FPGA chip, gives powerfull tools for calculations in parallel and pass through high-speed interfaces vast portions of data. This FPGA feature not only allows to perform processing of multiple data streams in real time but to synchronize these streams with high accuracy as well.

Attractive price, powerfull development tools, the possibility of multiple reprogramming, all this makes **uScio USB 3.0 FMC Carrier Board** the most appropriate tool for creating unique measurement software and hardware systems.



The FPGA, that is a base of the **uScio USB 3.0 FMC Carrier Board**, has huge computing performance. In order to uncover this feature to the full, **uScio USB 3.0 FMC Carrier Board** is equipped with modern high-speed interfaces. Widespread FMC ecosystem, promoted by Xilinx, provides a wide range of expansion cards. FMC boards range is constantly growing and can meet the requirements of modern scientific experiment.

## **uScio USB 3.0 FMC Carrier Board** has following features:

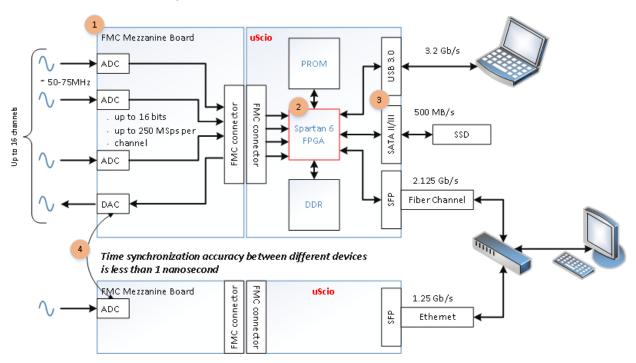
- FMC (LPC) connector. Designed for connection of any FMC mezzanine I / O board, which are compliant with the VITA 57 specification.
- Mode switch and programming SPI Flash. SPI Flash is designed to store executable RTL code for FPGA. FPGA automatically loads the code when powering up or pressing the "Reset FPGA».
- 3 SPI Flash programming connector. Intended for writing RTL code to SPI Flash.
- 4 UART connector (3.3v CMOS). Interface is connected to USB 3.0 controller.
- 5 ARM JTAG (20- pin) is designed for USB 3.0 controller debugging.
- 6 Programmable LED for indicating various events.
- 7 USB controller boot mode switch.
- 8 External programmable LEDs connector.
- 9 USB 3.0 connector (Type B). Allows data transferring to host computer on rate up to 3.2 Gbit/s.
- External power supply connector. Used in case the FMC mezzanine board has high power consumption.
- USB controller reset button.
- FPGA reset button.
- SFP connector. Designed to connect either Ethernet or Fiber Channel SFP modules. Communication speed when using SFP Ethernet module is up to 1.25 Gbit/s and Fiber Channel module is up to 2.125 Gbit/s.
- Two SATA II/III connectors. Designed to connect external HDD and/or SSD. Data transfer speed is up to 500 MB/s.
- xilinx Spartan6 LX150T FPGA (LX45T, LX100T optional).
- Xilinx FPGA JTAG connector. Intended for FPGA programming and RTL code debugging.

## **Using uScio USB 3.0 FMC Carrier Board**

In depends on task **uScio** could be connected to FMC expansion 1 board that has necessary functionality. For example, a multi-channel high-speed boards analog-to-digital and digital-to-analog converters allows to synchronously digitize signals from the antenna elements array or to prototype SDR (Software Defined Radio) systems. All the required information that needed to connect third-party developers FMC boards will be provided to **uScio** users.

The **uScio** functionality is completely determined by the RTL code (IP Core) running on <sup>2</sup> FPGA. Included in the **uScio SDK** IP Cores provide physical and program interfaces to all the hardware resources of the board. External DDR memory allows storing intermediate results of calculation. Executable RTL code can be stored in the PROM in order to FPGA automatically to be loaded after board power-up or reset FPGA.

Except high-speed data transfer between external interfaces FPGA resources allow embedding any others IP Cores that implement data processing algorithms. For example, hardware resources of FPGA Spartan 6 LX150 at a clock frequency 100-150 MHz allow posting either 22 a fast Fourier transform (1024 points) or 8 blocks convolution of two functions (with window 1024) or two-dimensional block 4 Fast Fourier Transform (256x256 points).



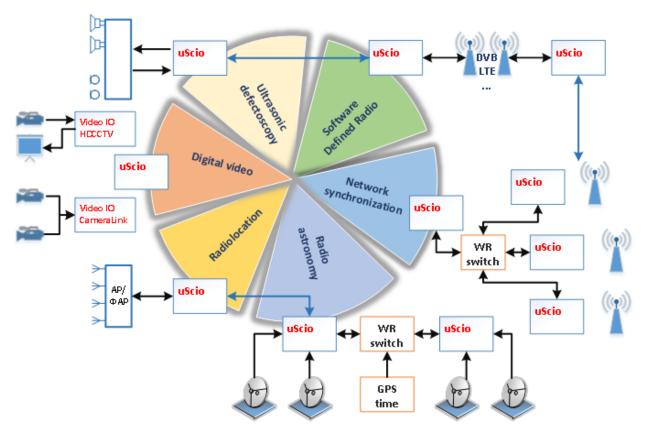
High-speed interfaces provide simple integration of the **uScio** board in the experimental equipment. Up to 3.2 Gbit/s any kind of data from FMC extension card can be uploaded directly to the

host computer for further tasks. USB and Ethernet / Fiber Channel can be used not just for transmission but also for the control board. If the bandwidth of USB or Ethernet is insufficient, data can be stored for later processing in the HDD/SSD.

**uScio** board allows synchronization to be up to 1 nanosecond when all network components support White Rabbit technology. 4

## **Application uScio USB 3.0 FMC Carrier Board**

**uScio** has a unique versatile functionality that can be used to develop test benches, research and experimental systems of any complexity.



On the purchase card, please contact sales@minerva-tech.com

Advice on technical issues please contact – <u>tsup@minerva-tech.com</u>